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Electroplasticity Memory Devices using Conducting Polymers and Solid Polymer Electrolytes*

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Abstract: Erasable memory devices are fabricated by the combination of a conducting polymer and solid polymer electrolyte. The former is used as a memory channel and the latter as an electrolyte medium. The channel conductivity can be controlled over 3–4 orders of magnitude by electrochemical doping through a writing electrode. The response time, depending on the writing voltage, is several seconds. The characteristics of the memory device are discussed.

Key words: erasable memory, transistor, conducting polymer, solid polymer electrolyte, doping.

INTRODUCTION

Conducting polymers (CPs) are of interest for the following reasons. The CPs are quasi-one-dimensional semiconductors with a highly conjugated π electron system.[1,2] The electrical conductivity is varied by the level of oxidation or reduction.[1,2] This can be achieved by an electrochemical method, in which the applied voltage between the CP and a counter electrode in an electrolyte medium determines the level of oxidation. Many applications of CPs have been tried for electronic devices such as diodes,[3] field effect transistors[4] using semiconductive features. Rechargeable batteries[5,6] and color switching cells[7] have also been examined for their electrochemical processes. However, except for the batteries,[6] none of them have been developed to the stage of practical use.

Recently, solid polymer electrolytes (SPE)[8] have been studied intensively and improved in their ionic conductivities. Since the SPE is a dry electrolyte, the SPE makes it possible for the electrochemical process to be used for microelectrochemical devices.[9] It is expected that by combining CP and SPE electrically erasable memory devices can be fabricated.[10] In these devices, the memory channel consists of CP, whose conductivity is controlled by the electrochemically-injected or -released charges through a writing electrode. Furthermore, the channel conductivity remains constant on opening the writing circuit. This analogue memory device with an electroplasticity function may be similar to the synapse connection in neural networks.

In this paper, the fabrication method and characteristics of the erasable memory device using CP and SPE are reported. The response times of the device for various types of the construction are discussed.

2 EXPERIMENTAL

2.1 Fabrication of memory devices

For the construction of the memory devices, a three-electrode structure was adopted. These electrodes were source, drain and gate (writing electrode) similar to the usual field effect transistors. Two types of the structure were fabricated, namely, a plane type and a layer type, which differed in the configuration of the memory channel.

Figures 1(a) and (b) show the schematic drawings of the

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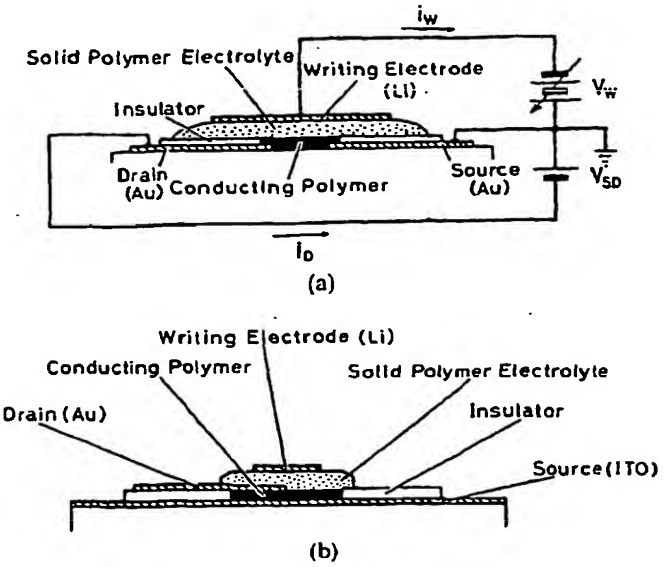

Fig. 1. The schematic drawing of the fabricated memory devices. (a) Planar type and the measuring circuit; (b) the layer type.

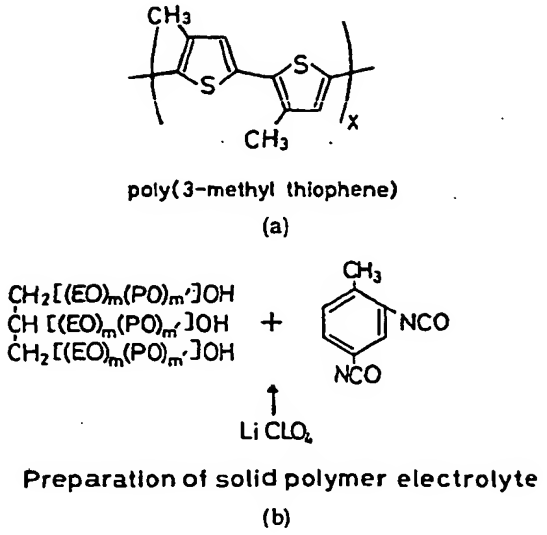

Fig. 2. (a) The molecular structure of poly(3-methylthiophene); (b) molecular structures of the solid polymer electrolyte.

planar type and the layer type, respectively. For the planar type, Au was deposited *in vacuo* on a glass plate with an area of 1 mm × 15 mm and thickness of *c.* 100 nm. The Au thin films, which were the source and drain electrodes, were separated by a gap with a distance of about 10 μm. The photoresisting material of EFPO from Tokyo Kasei Co. Ltd, was coated by a spinner onto the Au electrodes. The photoresisting material at the ends of the electrode and the gap, was irradiated with ultraviolet light and etched with organic solvents. The reset of photoresisting material, as shown in Fig. 1(a), was carried out by heat treatment at 200°C for 3 h and was used as the insulator.

A conducting polymer of poly(3-methylthiophene) shown in Fig. 2(a) was electrochemically deposited at the gap using a syringe with an electrolyte of *c.* 0·1 mol/liter 3-methylthiophene and 1 mol/liter $LiClO_4$ in benzonitrile after the method described in a previous paper.[2] The conductivity of CP deposited at the gap was simultaneously measured during the deposition. The polymerization was continued until the channel conductivity reached an appropriate value, e.g. *c.* 100Ω in resistance.

In the case of the layer type, one side of the glass substrate was covered with an Au thin film by vacuum deposition, followed by coating with the photoresisting material. The center of the photoresisting material was photo-etched in an area of 2 mm × 2 mm, at which the poly(3-methylthiophene) was electrochemically deposited to a thickness of several μm.

After the deposition of CP for the both types, the electrolyte solution was rinsed away with acetonitrile. A co-poly(ethylene oxide-propylene oxide), shown in Fig. 2(b), was used as the matrix of SPE. 4-Methyl-1,3-phenylene diisocyanate (T. Ohsawa and S. Yoneyama, pers. comm.) and $LiClO_4$ were used as a crosslinking agent and electrolyte, respectively. The mixture of these materials, dissolved in methyl ethyl ketone, was painted on the top of CP films as shown in Figs 1(a) and (b), followed by a heat treatment at *c.* 80°C for several minutes in order to solidify the SPE. A piece of Li foil 1 mm × 1 mm and 80 μm thickness was pressed on the top of SPE as the writing electrode.

2.2 Evaluation circuit of the devices

The evaluation circuit is shown in Fig. 1(a). The channel conductivity was measured by the drain current (i_D) at a constant voltage of $V_{SD} = 0{\cdot}2$ V applied across the source and drain electrodes. The i_D is proportional to the channel conductivity. The writing current of i_W was also measured to obtain the cyclic voltammetry by a linear sweep of the writing voltage (V_W). A similar circuit was used for the layer type device. In the writing process, negative voltages of V_W were applied across the source electrode, which induced an anion (ClO_4^-) doping in the CP. This resulted in an increase in channel conductivity. By shortening the writing and source electrodes, dopants were released and channel conductivity decreased to its original value.

3 RESULTS AND DISCUSSION

The cyclic voltammogram of the layer type memory device is depicted in Fig. 3(a), where V_W is the applied voltage against the writing electrode and i_W corresponds to the anodic or cathodic current. The sweep rates are indicated on the diagram. The hysteresis observed is the evidence for the Faraday current, i.e., electrochemical doping and undoping in the CP. Curves in Fig. 3(b) indicate the responses of the drain current versus V_W, which were obtained simultaneously in the experiment of cyclic voltammetry of Fig. 3(a).

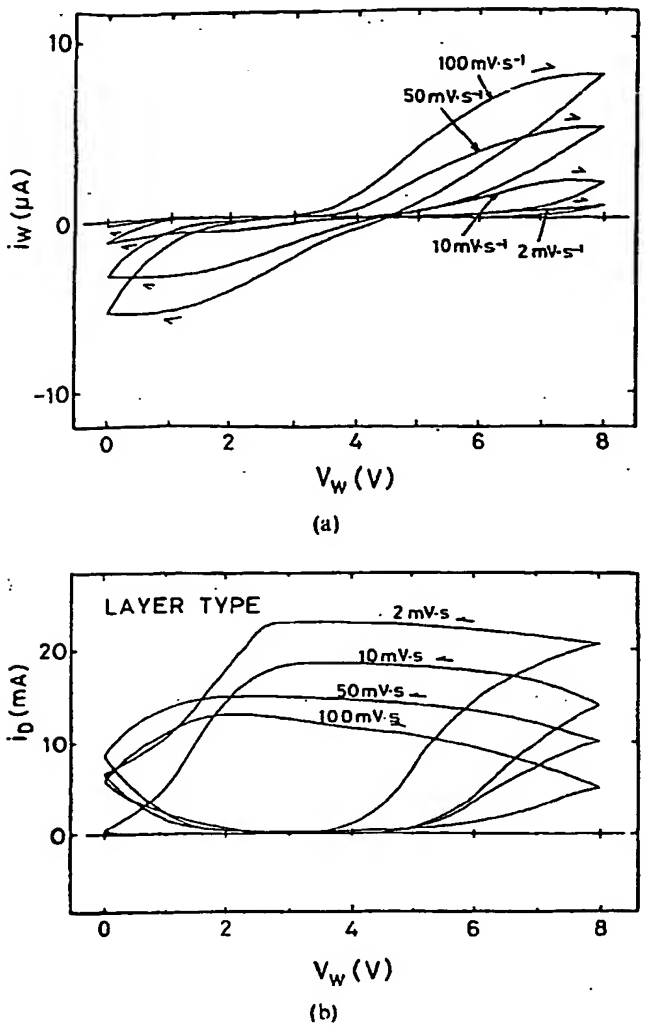

Fig. 3. Cyclic voltammogram of the memory device of the layer type. (a) The writing voltage versus the writing current; (b) the writing voltage against the drain current.

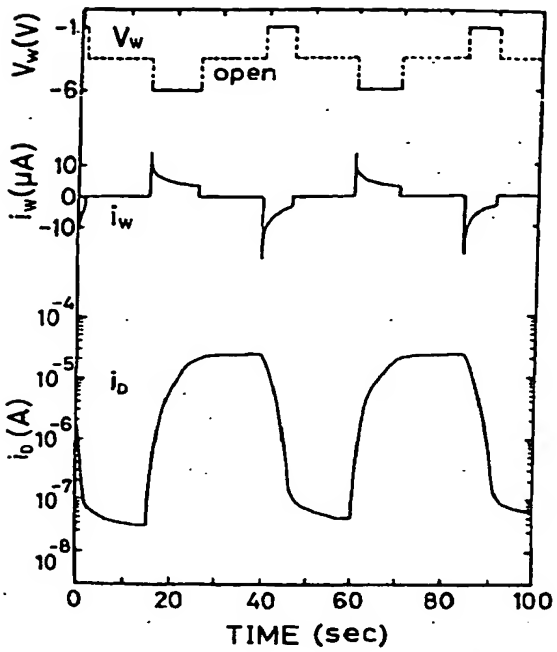

Fig. 4. Cyclic responses of the writing voltage (V_W), writing current (i_W) and drain current (i_D) for the planar type.

At the slow sweep, the i_D increased at a lower V_W and to a larger value compared with the rapid sweep. This indicates that the drift velocity of ions in the SPE or the ion transport at the interface of SPE and CP limited the rate of electrochemical doping.

Figure 4 shows the cyclic responses of V_W, i_W and i_D of the planar type cell, where i_D is plotted on a logarithmic scale. As evident, the conductivity of the memory channel varied by 3–4 orders of magnitude. In this experiment, V_W was applied as shown by the top curve in Fig. 4, namely, -6 V was applied for doping (writing) and -1 V for undoping (erasing) processes. At intervals the writing circuit was opened. From the i_W curve the doping level (about 1·5%) can be estimated for each cycle as mentioned in a previous paper.[10] This doping level is sufficient to reach a high conductive state.[2]

Figures 5(a) and (b) show the typical time responses for the planar type and layer type memory devices, respectively. These results indicate that rapid response is expected for the layer type. Namely, the switching time of the planar type was several seconds for the V_W of -5 V. On the other hand, that of layer type was 1–2 s. The i_W of the layer type was much larger than that of the planar type. However, the total charges injected during the writing were nearly the same. Holding of the memory state is less superior for the layer type. This may be due to the diffusion of dopant ions beneath the drain electrode as shown in Fig. 1(b). At the beginning, the doping should not occur under the drain electrode. The switching time was observed to be shorter for the application of a higher voltage of V_W, however, which resulted in the degradation of the polymer film.

A pulse operation of V_W for the writing process is shown in Fig. 6(a) for the planar type memory device. This result demonstrates that the channel conductivity increased stepwise at each pulse. A similar operation for the erasing process is shown in Fig. 6(b). The conductivity decreased stepwise with the erasing pulses. A good memory feature was observed, as shown by plateaus in Figs 6(a) and (b). The memory states lasted more than several hours. The level of memory can be changed by the number of pulsed signals applied positively or negatively. This indicates that the device can be used as a memory channel which is similar to a neural synapse connection with a learning effect function.

For the use of this memory device as an electronic circuit, a rapid response would be required. Reducing the channel distance and thickness may be effective for rapid response. It is also important to develop SPE with a higher ionic conductivity. The ion transport at the

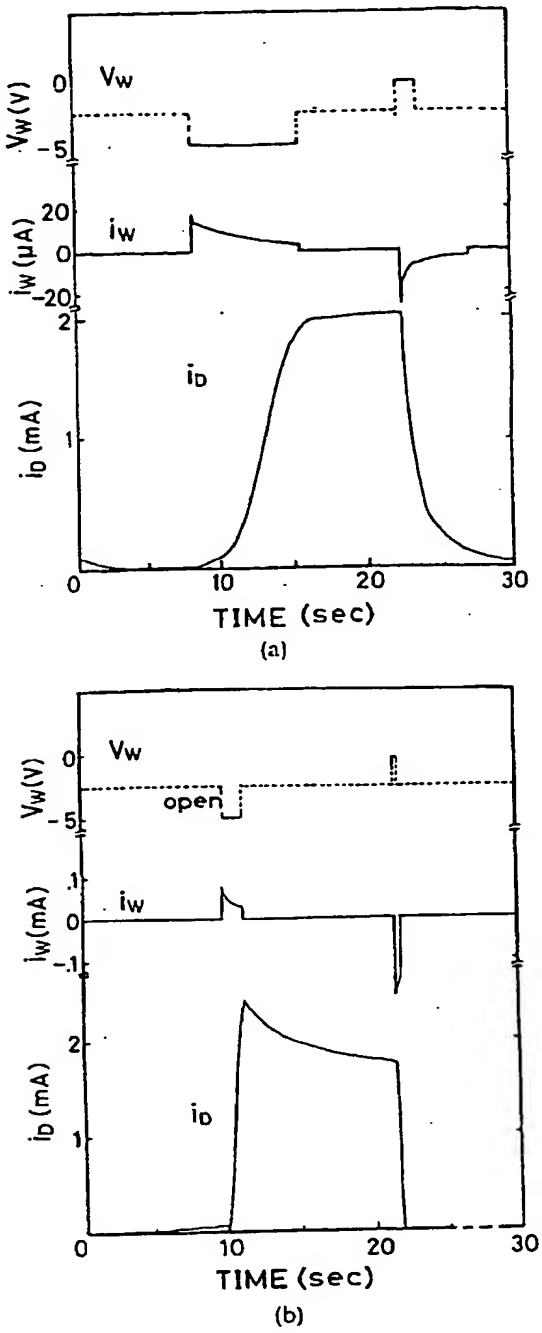

Fig. 5. Time responses of the V_W, i_W and i_D of the writing and erasing processes: (a) for the planar type and (b) for the layer type.

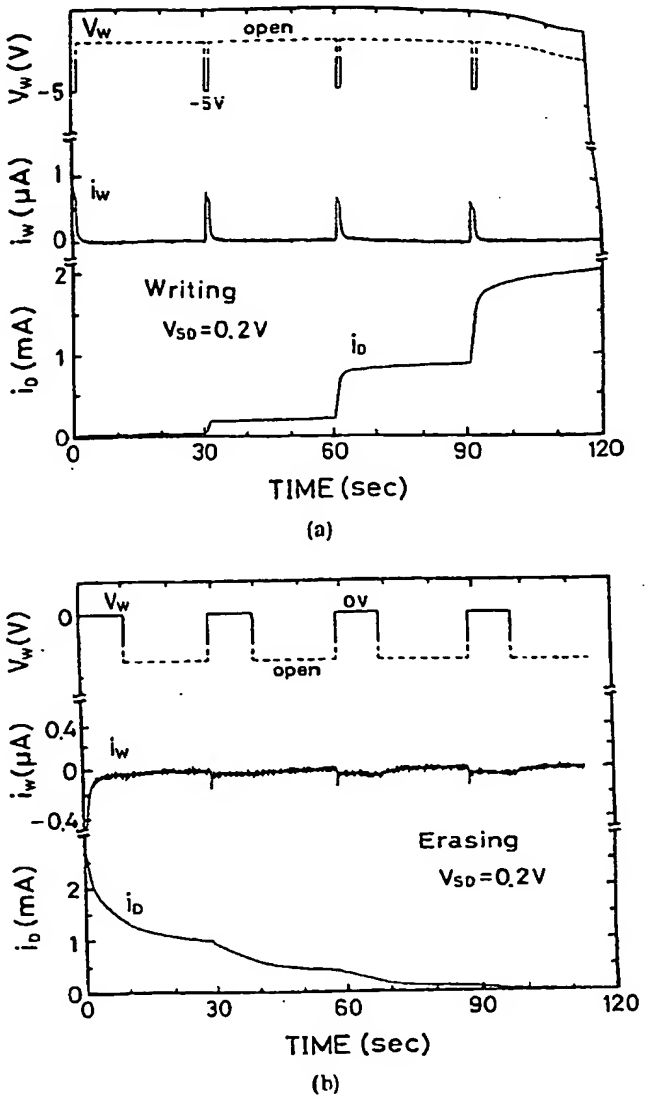

Fig. 6. Time responses of the V_W, i_W and i_D by the pulse operation of the planar type memory device: (a) for the writing and (b) for the erasing processes.

interface of the SPE and CP should also be subject to study. Various types of the memory device are being examined to achieve a more rapid response of the device.

4 CONCLUSIONS

Memory devices with electrically erasable functions were fabricated using a conducting polymer and a solid polymer electrolyte. The conducting polymer was used as a memory channel, whose conductivity was varied by 3–4 orders of magnitude by the application of a writing voltage of −5 V. The response time obtained was about 1–2 s for a layer type device. The pulse operation demonstrated that the device was useful as a digital/analogue converter for the input of serial pulses.

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